Call for Papers

Journal of Systems Architecture

Special Issue on

ON-CHIP PARALLEL & NETWORK-BASED SYSTEMS

General Scope

On-chip parallel and network-based system design to achieve functionality with low energy-speed product requires larger device count SoC design, multi block function design methodology, architectures and energy evaluation schemes. Such systems, which are emerging as the architecture of choice for future high performance processors, require high performance interconnects which are necessary to satisfy the data supply needs of all cores. This Special Issue is dedicated to research on on-chip communication technology, architecture, design methods and applications, bringing together research efforts of scientists and engineers working on on-chip innovations from related research communities, including parallel computer architecture, networking, and embedded systems. Original papers describing new and previously unpublished results are solicited on all aspects of on-chip parallel and networked system technology.

Topics

- On-chip network architecture (topology, routing, arbitration, ...)
- Network design for 3D stacked logic and memory
- Processor allocation and scheduling in CMPs
- Mapping of applications onto NoCs
- NoC reliability issues
- OS and compiler support for NoCs
- Performance and power issues in NoCs
- Metrics, benchmarks, and trace analysis for NoCs
- Multi/many-core workload characterization & evaluation
- Modeling and simulation of on-chip parallel and networked systems
- Synthesis, verification, debug & test of SoCs
- NoC support for memory and cache access
- SoC and NoC design methodologies and tools
- Network support for SoC Quality of Service (QoS)
- On-chip systems for FPGAs and structured ASICs
- NoC support for CMP/MPSocs
- Floorplan-aware NoC architecture optimization
- Application-specific NoC design
- Networked SoC case studies
- On-chip parallel programming models and tools
- Reconfigurable SoCs & NoCs
- Memory system design and optimizations for SoCs
- Early reports on system prototypes details
- SIMD parallel VLSI computing
- I/O interconnects and support for SoCs
- and other related topics…
Submission Information

All manuscripts and any supplementary material should be submitted via the online submission and peer review systems at http://ees.elsevier.com/jsa. Follow the submission instructions given on this site. Please select the article type as “PNB-SoCs”. All manuscripts should comply with the journal’s Guide for Authors. Please refer to the following site: http://www.elsevier.com/wps/find/journaldescription.cws_home/505616/authorinstructions.

Important Dates

Submission Deadline: 26 March 2010
Notification of Interim Decision: 26 May 2010
Revised Paper Submission: 10 June 2010
Final Decision: 20 July 2010
Final Paper: 10 August 2010

JSA Editor-in-Chief

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